

WHAT IS CLAIMED IS:

1           1.    Image processing circuitry, comprising:  
2                a two-dimensional image pipeline that is operable to  
3 process two dimensional image data to generate successive two-  
4 dimensional image frames for display in a two-dimensional image  
5 space;  
6                a three-dimensional image pipeline that is operable to  
7 process three-dimensional image data to render successive three-  
8 dimensional image frames for display in a two-dimensional image  
9 space; and  
10              dual mode sub-processing circuitry, associated with each  
11 of said two-dimensional image pipeline and said three-dimensional  
12 image pipeline, that is operable to perform motion compensation  
13 operations associated with said two-dimensional image pipeline in  
14 one mode and to perform rasterization operations associated said  
15 three-dimensional image pipeline in another mode.

1           2.    The image processing circuitry set forth in Claim 1  
2 wherein a portion of said dual mode sub-processing circuitry is  
3 further operable to sample reference frames in said one mode and to  
4 perform texture mapping in said another mode.

1 3. The image processing circuitry set forth in Claim 1  
2 wherein a portion of said dual mode sub-processing circuitry is  
3 further operable to blend samples from a plurality of reference  
4 frames in said one mode and to blend samples from a plurality of  
5 texture maps in said another mode.

1 4. The image processing circuitry set forth in Claim 2  
2 wherein a portion of said dual mode sub-processing circuitry is  
3 further operable to process said plurality of reference frames  
4 using error term in said one mode and to perform alpha blending in  
5 said another mode.

1 5. The image processing circuitry set forth in Claim 1 is  
2 operable to support at least one MPEG standard.

1 6. The image processing circuitry set forth in Claim 1  
2 further comprising an alpha blend sub-circuitry that is operable to  
3 process at least 8- and 9-bit signed values.

1        7. For use in image processing circuitry that comprises a  
2 two-dimensional image pipeline and a three-dimensional image  
3 pipeline, said two-dimensional image pipeline operable to process  
4 two dimensional image data to generate successive two-  
5 dimensional image frames for display in a two-dimensional image  
6 space, and said three-dimensional image pipeline operable to  
7 process three-dimensional image data to render successive three-  
8 dimensional image frames for display in a two-dimensional image  
9 space, a method of operating dual mode sub-processing circuitry  
10 that is associated with both of said pipelines, said method  
11 comprising the steps of:

12                performing motion compensation operations associated with  
13 said two-dimensional image pipeline in one mode; and

14                performing rasterization operations associated said  
15 three-dimensional image pipeline in another mode.

1        8. The method of operating said dual mode sub-processing  
2 circuitry set forth in Claim 7 further comprising the steps of:

3                sampling reference frames in said one mode; and

4                performing texture mapping in said another mode.

1 9. The method of operating said dual mode sub-processing  
2 circuitry set forth in Claim 7 further comprising the step of  
3 blending one of samples from a plurality of reference frames in  
4 said one mode and samples from a plurality of texture maps in said  
5 another mode.

1 10. The method of operating said dual mode sub-processing  
2 circuitry set forth in Claim 8 further comprising the steps of:  
3 processing said plurality of reference frames using error  
4 terms in said one mode; and  
5 performing alpha blending in said another mode.

1 11. The method of operating said dual mode sub-processing  
2 circuitry set forth in Claim 7 further comprising the step of  
3 switching from said another mode to said one mode to perform motion  
4 compensation in accordance with at least one MPEG standard.

1 12. The method of operating said dual mode sub-processing  
2 circuitry set forth in Claim 10 wherein said performing alpha  
3 blending step further comprising the step of processing at least 8-  
4 and 9-bit signed values.

1 13. The method of operating said dual mode sub-processing  
2 circuitry set forth in Claim 7 further comprising the step of  
3 controlling said dual mode sub-processing circuitry.

1 14. Mode control circuitry for use in an image processing  
2 system having a two-dimensional image pipeline that processes two  
3 dimensional image data to generate successive two-dimensional image  
4 frames and a three-dimensional image pipeline that is operable to  
5 process three-dimensional image data to render successive three-  
6 dimensional image frames, said mode control circuitry comprising:

7 dual mode sub-processing circuitry, associated with each  
8 of said two-dimensional and said three-dimensional image pipelines,  
9 that is operable to perform motion compensation operations  
10 associated with said two-dimensional image pipeline and to perform  
11 rasterization operations associated said three-dimensional image  
12 pipeline; and

13 a controller that is operable to control said dual mode  
14 sub-processing circuitry to perform said motion compensation  
15 operations in one mode and to perform said rasterization operations  
16 in said other mode.

1 15. The mode control circuitry set forth in Claim 14 wherein  
2 a portion of said dual mode sub-processing circuitry is further  
3 operable to sample reference frames in said one mode and to perform  
4 texture mapping in said other mode.

1 16. The mode control circuitry set forth in Claim 14 wherein  
2 a portion of said dual mode sub-processing circuitry is further  
3 operable to blend samples from a plurality of reference frames in  
4 said one mode and to blend samples from a plurality of texture maps  
5 in said other mode.

1 17. The mode control circuitry set forth in Claim 15 wherein  
2 a portion of said dual mode sub-processing circuitry is further  
3 operable to process said plurality of reference frames using error  
4 terms in said one mode and to perform alpha blending in said other  
5 mode.

1 18. The mode control circuitry set forth in Claim 14 wherein  
2 said dual mode sub-processing circuitry is operable to support at  
3 least one MPEG standard.

1 19. The mode control circuitry set forth in Claim 14 further  
2 comprising an alpha blend sub-circuitry that is operable to process  
3 at least 8-bit and 9-bit signed values.

1 20. For use in image processing circuitry that comprises a  
2 two-dimensional image pipeline and a three-dimensional image  
3 pipeline, said two-dimensional image pipeline operable to process  
4 two dimensional image data to generate successive two-  
5 dimensional image frames for display in a two-dimensional image  
6 space, and said three-dimensional image pipeline operable to  
7 process three-dimensional image data to render successive three-  
8 dimensional image frames for display in a two-dimensional image  
9 space, a method of operating mode control circuitry that is  
10 associated with both of said pipelines, said method comprising the  
11 step of controlling dual mode sub-processing circuitry to at least  
12 one of perform motion compensation operations associated with said  
13 two-dimensional image pipeline in one mode, and perform  
14 rasterization operations associated said three-dimensional image  
15 pipeline in another mode.

1 21. The method of operating mode control circuitry set forth  
2 in Claim 20 further comprising the steps of:  
3 sampling reference frames in said one mode; and  
4 performing texture mapping in said other mode.

1 22. The method of operating mode control circuitry set forth  
2 in Claim 20 further comprising the steps of:  
3 blending samples from a plurality of reference frames in  
4 said one mode; and  
5 blending samples from a plurality of texture maps in said  
6 other mode.

1 23. The method of operating mode control circuitry set forth  
2 in Claim 21 further comprising the steps of:  
3 processing said plurality of reference frames using error  
4 terms in said one mode; and  
5 performing alpha blending in said other mode.

1 24. The method of operating mode control circuitry set forth  
2 in Claim 20 wherein said dual mode sub-processing circuitry is  
3 operable to support at least one MPEG standard.



1 25. The method of operating mode control circuitry set forth  
2 in Claim 20 further comprising an alpha blend sub-circuitry that is  
3 operable to process at least 8-bit and 9-bit signed values.

1 26. A media processing system having a central processing  
2 unit, a memory subsystem, an image processing system, and a display  
3 system, said media processing system comprising:

4 a two-dimensional image pipeline that is operable to  
5 process two dimensional image data to generate successive two-  
6 dimensional image frames for display in a two-dimensional image  
7 space of said display system;

8 a three-dimensional image pipeline that is operable to  
9 process three-dimensional image data to render successive three-  
10 dimensional image frames for display in a two-dimensional image  
11 space of said display system; and

12 dual mode sub-processing circuitry, associated with each  
13 of said two-dimensional image pipeline and said three-dimensional  
14 image pipeline, that is operable to perform motion compensation  
15 operations associated with said two-dimensional image pipeline in  
16 one mode and to perform rasterization operations associated said  
17 three-dimensional image pipeline in another mode.